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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,534	04/12/2004	James D. Kelly	BP3249	3346

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EXAMINER	
SURYAWANSHI, SURESH	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 08/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,534	KELLY, JAMES D.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Bates et al (US Patent 6,711,696; hereinafter Bates).

4. As per claim 1, Bates discloses an apparatus comprising:

a first clock domain to operate at a first clock frequency [col. 4, lines 20-24, 53-58; 1GHz signal is referred to as the first signal];

a second clock domain to operate at a second clock frequency [col. 4, lines 20-24, 53-58; 800 MHz signal is referred to as the second signal]; and

an interface disposed between the first and second clock domains to control timing of data transfer from one of the first or second clock domains to other of the first or second clock domains, the interface to allow for a frequency ratio between the first and second clock domains which is not an integer ratio [col. 3, lines 12-16; col. 4, lines 20-24; col. 8, lines 1-3; transferring data from a first clock domain to a second clock domain wherein the clock rates or frequency of the domains are different and are not constrained to be integer or half-integer multiples of each other].

5. As per claim 9, Bates discloses an integrated circuit comprising:

a first clock domain to operate at a first clock frequency [col. 4, lines 20-24, 53-58; 1GHz signal is referred to as the first signal];

a second clock domain to operate at a second clock frequency [col. 4, lines 20-24, 53-58; 800 MHz signal is referred to as the second signal]; and

an interface disposed between the first and second clock domains to control timing of data transfer in both directions between the first clock domain and the second clock domain, the interface to allow for a frequency ratio between the first and second clock domains which is not an integer ratio [col. 3, lines 12-16; col. 4, lines 20-24; col. 8, lines 1-3; transferring data from a first clock domain to a second clock domain wherein the clock rates or frequency of the domains are different and are not constrained to be integer or half-integer multiples of each other].

6. As per claim 15, Bates discloses a method comprising:

generating a first clock signal having a first frequency to a first clock domain [col. 4, lines 20-24, 53-58; 1GHz signal is referred to as the first signal];

generating a second clock signal having a second clock frequency to a second clock domain, a ratio between the first clock frequency to the second clock frequency being a non-integer ratio [col. 4, lines 20-24, 53-58; 800 MHz signal is referred to as the second signal]; and

using an interface disposed between the first and second clock domains to control timing of data transfer from the first clock domain to the second clock domain, the interface made programmable to set a particular frequency ratio based on ratio of the first clock frequency to the second clock frequency [col. 3, lines 12-16; col. 4, lines 20-24; col. 8, lines 1-3; transferring data from a first clock domain to a second clock domain wherein the clock rates or frequency of the domains are different and are not constrained to be integer or half-integer multiples of each other].

7. As per claim 2, Bates discloses that the interface is made programmable to allow selection of different frequency ratios to be selected between the first and second clock domains [col. 4, lines 20-24; inherent to the system as the clock rates or frequencies of the domains are not constraint to be integer or half-multiples of each other].

8. As per claim 3, Bates discloses that the interface is to allow for a granularity of 0.25 in the frequency ratio between the first and second clock domains [col. 4, lines 20-24; inherent to the system as the clock rates or frequencies of the domains are not constraint to be integer or half-multiples of each other].

9. As per claims 4, 10 and 16, Bates discloses that the first clock domain is a bus domain and the second domain is a circuit operably coupled to the bus domain [col. 2, lines 31-50].

10. As per claim 5, Bates discloses that the interface to allow for data transfer in both directions in which first domain operates at a faster frequency than the second domain [col. 4, lines 20-24].

11. As per claims 6 and 14, Bates discloses that the interface includes a control circuit to set the frequency ratio and at least one latching circuit to latch data through the interface from one clock domain to the other clock domain [col. 4, lines 20-24; inherent to the system as the clock rates or frequencies of the domains are not constraint to be integer or half-multiples of each other].

12. As per claim 7, Bates discloses including a plurality of latching circuits, in which separate latching circuits are to be used to transfer data in a particular direction between the first and second clock domains [col. 4, lines 20-24; inherent to the system for transferring data from a first clock domain to a second clock domain].

13. As per claim 8, Bates discloses that the control circuit of the interface further includes a first and second ratio generators in which the first ratio generator is to be used to generate control signals to the latching circuits, if the ratio difference is below a particular ratio and the second ratio generator is to be used to generate control signals to the latching circuits if the ratio difference is equal to or above the particular ratio [col. 4, lines 20-24; inherent to the system for transferring data from a first clock domain to a second clock domain wherein the clock rates or frequencies of the domains are not constrained to be integer or half-integer multiples of each other].

14. As per claim 11, Bates discloses that the first and second domains are synchronized from a same clock source, but in which the first domain operates at a faster clock frequency than the second domain [col. 4, lines 50-58].

15. As per claims 12 and 17, Bates discloses that the interface is to allow for a frequency ratio of N:4, where N is an integer, to have a granularity 0.25 for the frequency ratio between the first and second clock domains [col. 4, lines 20-24; inherent to the system as the clock rates or frequencies of the domains are not constraint to be integer or half-multiples of each other].

16. As per claims 13 and 18, Bates discloses including a plurality of additional clock domains operably coupled to the bus domain and in which a separate interface is disposed between the bus domain and the additional domains, the interfaces made programmable to allow selection of different frequency ratios to be selected between the bus domain and the additional domains [col. 2, lines 31-50; col. 4, lines 20-24; inherent to the system as the clock rates or frequencies of the domains are not constraint to be integer or half-multiples of each other].

17. As per claim 19, Bates discloses including latching data from the bus domain to the second domain by counting a difference in the clock pulses based on the particular frequency ratio and skipping certain ones of excess clock pulses to have a one-to-one data transfer timing between the two clock domains [col. 3, lines 33-39; col. 4, lines 20-24; inherent to the system for transferring data from a first clock domain to a second clock domain].

18. As per claim 20, Bates discloses including latching data from, the bus domain to the second domain by counting a difference in the edges based on the particular frequency ratio and skipping certain ones of excess clock edges to have a one-to-one data transfer timing between the two clock domains [col. 3, lines 33-39; col. 4, lines 20-24; inherent to the system for transferring data from a first clock domain to a second clock domain].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

sks
July 24, 2006

THOMAS LEE
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